Listing of the Claims:

Claim 1 (Currently amended): A semiconductor device, comprising:

a semiconductor substrate;

an isolation layer formed on the semiconductor substrate for defining a plurality of active regions, each of the plurality of active regions having a major axis and a minor axis;

a plurality of gates formed to cross the plurality of active regions and extend in a direction of the minor axis of each of the plurality of active regions, each of the plurality of gates having a first side and a second side that are opposing and that run along the direction of the minor axis;

a plurality of first and second source/drain regions formed in the plurality of active regions at either of the first side or the second side of each of the plurality of gates, each of the plurality of first and second source/drain regions having a top surface;

a plurality of first self-aligned contact pads (SACs) and a plurality of second SACs formed to contact the top surface of each of the plurality of first and second source/drain regions, respectively, and wherein the plurality of first SACs ~~self-aligned contact pads~~ and the plurality of second SACs have ~~are~~ substantially the same ~~size~~ top surface area.

Claim 2 (Original): The semiconductor device of claim 1, wherein the plurality of gates are formed such that each two of the plurality of gates crosses one of the plurality of active regions.

Claim 3 (Original): The semiconductor device of claim 1, wherein the isolation layer has a top surface, and said semiconductor device further comprises a plurality of third SACs formed

to contact areas of the top surface of the isolation layer that are disposed between adjacent first SACs in a direction of the major axis of each of the plurality of active regions.

Claim 4 (Currently amended): The semiconductor device of claim 1, wherein each of the plurality of second SACs have sidewalls and a top surface, the isolation layer has a top surface, an arrangement of the plurality of second SACs forms a plurality of columns, an arrangement of the plurality of first SACs and the plurality of second SACs forms a plurality of first rows having a plurality of second rows disposed in an alternating arrangement there between to isolate each of the plurality of first rows from one another, and the semiconductor device further comprises:

a plurality of contact plugs, each of the plurality of contact plugs having a top surface, each of the plurality of contact plugs formed to contact the sidewalls and a predetermined portion of the top surface of one of the plurality of second SACs and a portion of the top surface of the isolation layer, and wherein each of the plurality of contact plugs is positioned along one of the plurality of columns corresponding to one of the arrangements of the plurality of the second SACs; and

a plurality of bit lines, wherein each of the plurality of bit lines are formed to contact the top surface of at least one of the plurality of contact plugs and extends in a direction of the major axis along the plurality of second rows where there is an absence of the plurality of active regions.

Claim 5 (Original): The semiconductor device of claim 4, wherein each of the plurality of contact plugs has sidewalls and a bottom surface, and said semiconductor device further

comprises a metal barrier layer formed to surround the sidewalls and the bottom of each of the plurality of contact plugs.

Claim 6 (Original): The semiconductor device of claim 5, wherein the metal barrier layer is formed of a double layer comprising a Ti layer and a TiN layer.

Claim 7 (Original): The semiconductor device of claim 4, wherein each of the plurality of bit lines comprises a stacked body having a conductive recess-prevention layer, a bit line conductive layer, a bit line capping layer, sidewalls, and bit line spacers formed to surround the sidewalls of the stacked body.

Claim 8 (Original): The semiconductor device of claim 7, wherein the conductive recess prevention layer is formed of a double layer comprising a Ti layer and a TiN layer.

Claim 9 (Previously amended): The semiconductor device of claim 4, further comprising:

a plurality of third SACs, each of the plurality of third SACs having sidewalls and a top surface, and formed to respectively contact areas of the top surface of the isolation layer that are positioned along a same vertical axis as the plurality of first and second source/drain regions, wherein each of the plurality of contact plugs is formed to further contact the sidewalls and a predetermined portion of the top surface of one of the plurality of third SACs positioned along the same column as one of the plurality of second SACs, respectively.

Claim 10 (Cancel):

Claim 11 (Currently amended): A method for manufacturing a semiconductor device, comprising the steps of:

forming an isolation layer on a semiconductor substrate, the isolation layer for defining a plurality of active regions, each of the plurality of active regions having a major axis and a minor axis;

forming a plurality of gates on areas of the semiconductor substrate on which the isolation layer is formed, the plurality of gates formed to cross the plurality of active regions and extend in a direction of the minor axis of each of the plurality of active regions, each of the plurality of gates having a top surface and having a first side and a second side that are opposing and that ~~that~~ run along the direction of the minor axis;

forming a plurality of first and second drain/source regions in the plurality active regions at either of the first side or the second side of each of the plurality of gates, each of the plurality of first and second source/drain regions having a top surface;

forming a first interlayer insulating layer on regions of the semiconductor substrate on which the plurality of first and second source/drain regions are formed, the first interlayer insulating layer formed to completely fill spaces among the plurality of gates and to have a planarized top surface;

forming photoresist patterns in a line shape at each of a plurality of rows where there is an absence of any formation of the plurality of active regions on the first interlayer insulating layer, the line shape extending in a direction of the major axis;

etching the first interlayer insulating layer using the photoresist patterns as etching masks to form a plurality of contact holes through which the top surface of each of the plurality of first and second source/drain regions are respectively exposed;

removing the photoresist patterns; and

forming a plurality of first self-aligned contact pads (SACs) and a plurality of second SACs to respectively contact the top surface of each of the plurality of first and second source/drain regions and to be level with the top surface of each of the plurality of gates, by filling the plurality of contact holes with a conductive material.

Claim 12 (Original): The method of claim 11, wherein the plurality of gates are formed such that each two of the plurality of gates crosses one of the plurality of active regions.

Claim 13 (Original): The method of claim 11, wherein said step of forming the plurality of gates comprises the steps of:

sequentially forming a gate insulating layer, a gate electrode, and a capping layer on the areas of the semiconductor substrate on which the isolation layer is formed;

patterning the gate insulating layer, the gate electrode, and the capping layer to form a patterned gate insulating layer, a patterned gate electrode, and a patterned capping layer; and

forming gate spacers to surround sidewalls of the patterned gate insulating layer, the patterned gate electrode, and the patterned capping layer,

wherein the capping layer and the gate spacers are formed of an insulating material having a different etching selectivity from that of the first interlayer insulating layer.

Claim 14 (Original): The method of claim 11, further comprising the step of forming a material layer that partially fills the spaces among the plurality of gates, subsequent to said step of forming the plurality of first and second source/drain regions,

wherein the material layer is formed of an insulating layer having a different etching selectivity from that of the first interlayer insulating layer and is etched along with the first interlayer insulating layer.

Claim 15 (Previously amended): The method of claim 11, wherein each of the plurality of the second SACs has sidewalls and a top surface, the isolation layer has a top surface, an arrangement of the plurality of second SACs forms a plurality of columns, an arrangement of the plurality of first SACs and the plurality of second SACs forms a plurality of first rows having a plurality of second rows disposed in an alternating arrangement there between to isolate each of the plurality of first rows from one another, and said method further comprises the steps of:

forming a second interlayer insulating layer on portions of the semiconductor substrate on which the plurality of first SACs and the plurality of second SACs are formed;

forming a plurality of contact plugs through the first and the second interlayer insulating layers to respectively contact the sidewalls and a predetermined portion of the top surface of each of the plurality of second SACs and a portion of the top surface of the isolation layer, wherein each of the plurality of contact plugs are positioned along a same column as one of the arrangements of the plurality of second SACs; and

forming a plurality of bit lines, wherein each of the plurality of bit lines are formed along one of the plurality of second rows and extends in a direction of the major axis of each of the

plurality of active regions, and wherein the plurality of second rows are formed where there is an absence of the plurality of active regions.

Claim 16 (Previously amended): The method of claim 15, wherein said step of forming the plurality of contact plugs comprises the steps of:

etching the first and second interlayer insulating layers to form a plurality of contact holes, wherein each of the plurality of contact holes is formed to respectively expose there through the sidewalls and the predetermined portion of the top surface of one of the plurality of second SACs, and wherein the portion of the top surface of the isolation layer is positioned at the same one of the plurality of columns as the one of the plurality of second SACs and at one of the plurality of second rows that precedes or follows one of the plurality of first rows within which lies the one of the plurality of second SACs;

forming a conductive layer to completely fill each of the plurality of contact holes; and

planarizing a top surface of the conductive layer to expose a top surface of the second interlayer insulating layer.

Claim 17 (Original): The method of claim 15, further comprising the step of forming a barrier metal layer at sidewalls and a bottom surface of each of the plurality of contact holes, subsequent to said step of etching the first and second interlayer insulating layers.

Claim 18 (Original): The method of claim 17, wherein the barrier metal layer is formed of a double layer consisting of a Ti layer and a TiN layer.

Claim 19 (Original): The method of claim 15, further comprising the step of forming a plurality of third SACS to respectively contact the top surface of the isolation layer positioned along a same horizontal axis as the plurality of first and second source/drain regions,

wherein each of the plurality of contact plugs is formed to further contact sidewalls and a predetermined portion of each of the plurality of third SACs positioned at the same column as the one of the plurality of second SACs.

Claim 20 (Original): The method of claim 15, wherein the step of forming the plurality of bit lines comprises the steps of:

sequentially forming a conductive recess prevention layer, a bit line conductive layer, and a bit line capping layer on areas of the semiconductor substrate on which the plurality of contact plugs are formed;

patterning the conductive recess prevention layer, the bit line conductive layer, and the bit line capping layer to obtain a patterned conductive recess prevention layer, a patterned bit line conductive layer, and a patterned bit line capping layer; and

forming bit line spacers to surround sidewalls of the patterned conductive recess prevention layer, the patterned bit line conductive layer, and the patterned bit line capping layer.

Claim 21 (Original): The method of claim 20, wherein the conductive recess prevention layer is formed of a double layer consisting of a Ti layer and a TiN layer.

Claim 22 (Previously amended) The method of claim 11, wherein each of the photoresist patterns are formed to include a protrusion covering the top surface of the isolation layer positioned at each of a plurality of rows where the plurality of active regions are formed.

Claim 23 (Previously amended): The method of claim 22, wherein the protrusion covering the top portion of the isolation layer positioned at each of the plurality of rows where the active regions are formed is formed to extend over any of the plurality of gates.